Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A serial data mapping apparatus, comprising:

an STM-1 address generating unit that generates a mapping address;

a VC mapping unit that maps a DS asynchronous signal to a VC signal as a byte unit, according to the mapping address; and

an STM-1 formatter that pointer processes and multiplexes a virtual container of the mapped VC signal and generates an STM-1 signal,

wherein the VC mapping unit comprises a plurality of elastic buffers that write the DS asynchronous signal as a bit unit and read the DS asynchronous signal as the byte unit comprising a parallel asynchronous signal of 8 bits.

2. (Currently Amended) The apparatus of claim 1, wherein the VC mapping unit further comprises:

~~a plurality of elastic buffers that write the DS asynchronous signal as a bit unit and read the DS asynchronous signal as the byte unit;~~

a write pointer generating unit that generates write addresses for the plurality of elastic buffers;

a read pointer ~~controlling~~ generating unit that generates read addresses for the plurality of elastic buffers;

a VC1 mapper that multiplexes parallel asynchronous data of the byte unit, read in the respective elastic buffers, into the VC signal according to a format controlling signal; and

a VC1 framer that identifies a mapping position of the DS asynchronous signal, according to the mapping address outputted from the STM-1 address generating unit, and controls the elastic buffers, the read pointer ~~controlling~~ generating unit, and the VC1 mapper according to the identified mapping position.

3. (Original) The apparatus of claim 1, further comprising:

a plurality of elastic buffers that write the DS asynchronous signal as a bit unit and read the DS asynchronous signal as the byte unit,

the plurality of elastic buffers writes the DS asynchronous signal by being synchronized to a system clock signal.

4. (Currently Amended) The apparatus of claim 2, wherein the read pointer ~~controlling~~ generating unit outputs a start bit of the byte unit as the read address, ~~by controlling the read pointer generating unit~~.

5. (Currently Amended) The apparatus according to claim 4, wherein the read pointer ~~controlling~~ generating unit outputs the read address as increased by +8, +6, or +4 according to the mapping position identified by the VC1 framer.

6. (Currently Amended) A serial data mapping apparatus, comprising:

a plurality of elastic buffers, each buffer receiving serial asynchronous data, and outputting parallel data bits as byte units of the asynchronous data; and

a virtual container mapping unit that receives the ~~parallel data bits~~byte units from the plurality of elastic buffers and maps the ~~parallel data bits~~byte units to a virtual container signal.

7. (Original) The serial data mapping apparatus of claim 6, further comprising an STM-1 formatter that multiplexes the virtual container signal as an STM-1 signal.

8. (Currently Amended) The serial data mapping apparatus of claim 6, further comprising:

an STM-1 address generating unit that generates a mapping address;

a virtual container multiplexer, within the virtual container mapping unit, that multiplexes a number of the ~~parallel data bits~~ byte units received from the plurality of elastic buffers into the virtual container; and

a virtual container framer that identifies a mapping position of the asynchronous signal, based on the mapping address generated by the STM-1 address generating unit, and controls the multiplexing of the number of ~~parallel data bits~~byte units into the virtual container.

9. (Currently Amended) A ~~The~~ serial data mapping apparatus ~~of claim 6,~~ comprising:

a plurality of elastic buffers, each buffer receiving serial asynchronous data, and outputting parallel data bits of the asynchronous data; and

a virtual container mapping unit that receives the parallel data bits from the plurality of elastic buffers and maps the parallel data bits to a virtual container signal,

wherein the virtual container mapping unit further comprises:

a read pointer generating unit that generates the read addresses for the plurality of elastic buffers, and wherein

the read pointer generating unit generates the read address of a start bit of the parallel data bits,

the read pointer generating unit increments or decrements the read address, after each of a number of the parallel data bits is read from the elastic buffer, by a value of four, six, or eight, and

the value by which the read pointer generating unit is incremented or decremented depends on a number of null bits received in the serial asynchronous data corresponding to the parallel data bits read from the elastic buffer.

10. (Original) The serial data mapping apparatus of claim 6, further comprising a system clock that controls the timing of writing the asynchronous data to the plurality of elastic buffers and reading the parallel data bits from the plurality of elastic buffers to the virtual container mapping unit.

11. (Original) The serial data mapping apparatus of claim 6, further comprising:

an STM-1 formatter that multiplexes the virtual container signal as an STM-1 signal; and

a read pointer generating unit that generates the read addresses for a plurality of DS-1 signals and a plurality of DS-1E asynchronous signals received by the plurality of elastic buffers, wherein

the virtual container mapping unit maps portions of the plurality of DS-1 and DS-1E signals into the virtual container signal, and

the STM-1 formatter multiplexes the virtual container having the portions of the DS-1 and DS-1E signals into the STM-1 signal.

12. (Original) The serial data mapping apparatus of claim 11, further comprising a system clock that controls the timing of writing the asynchronous data to the plurality of elastic buffers and reading the portions of the plurality of DS-1 and DS-1E signals from the elastic buffer to the virtual container mapping unit.

13. (Currently Amended) A method of mapping serial data ~~mapping~~, comprising:

receiving each of a plurality of serial asynchronous data signals into a plurality of elastic buffers, respectively;

reading a parallel asynchronous signal of 8 bits as a parallel data byte unit;

multiplexing parallel data units read from the plurality of elastic buffers into a virtual container signal~~, each parallel data unit containing multiple data bits read in parallel;~~ and

generating an STM-1 signal from the virtual container signal.

14. (Original) The method of claim 13, further comprising:

reading the parallel data units from the plurality of elastic buffers, according to generated read addresses; and

writing the plurality of serial asynchronous data signals to the plurality of elastic buffers, according to generated write addresses; wherein

a system clock controls the timing of writing the serial asynchronous data to the plurality of elastic buffers and reading the parallel data unit from the plurality of elastic buffers to the virtual container signal.

15. (Original) The method of claim 13, wherein a number of read pointer generating units, which each generate a read address for a number of the respective plurality of elastic buffers, is less than the number of elastic buffers in the plurality of elastic buffers.

16. (Original) The method of claim 13, wherein a number of write pointer generating units, which each generate a write address for a number of the respective plurality of elastic buffers, is less than the number of elastic buffers in the plurality of elastic buffers.